AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 10 and 20 without prejudice and amend claim 7 as follows:

LISTING OF CLAIMS:

1. (Previously Presented) A data processing system comprising:

a plurality of processors for executing a series of different types of processing functions on data to be processed in a prescribed order, each processor executing a processing function different from one another and said data to be processed being image data that consists of a plurality of pixel data; and

a memory for storing said data to be processed in association with state information to represent the processing to be performed next for each pixel data of said data to be processed, wherein

said processing functions are asynchronously executed on said data to be processed by said plurality of processors, one processing is executed on each pixel data by one of the processors at a time and said plurality of processors share said memory.

2. (Original) The data processing system according to claim 1, wherein

said plurality of processors each determine if said data to be processed can be processed based on said state information.

3. (Previously Presented) The data processing system according to claim 2, wherein

said plurality of processors each execute a processing on said data to be processed, and then rewrite said state information corresponding to the processed data.

4. (Previously Presented) The data processing system according to claim 1, further comprising a first controller for controlling said plurality of processors to execute said series of processing functions based on said state information.

5. (Previously Presented) The data processing system according to claim 4, wherein

said first controller rewrites said state information corresponding to processed data in response to the completion of each processing by said plurality of processors.

6. (Previously Presented) The data processing system according to claim 1, further comprising a second controller for determining an attribute of said data to be processed, wherein

said second controller rewrites said state information corresponding to said data to be processed in order to change the order of executing said series of processing functions if it is determined that said data to be processed has a prescribed attribute.

7. (Currently Amended) The data processing system according to claim 6, wherein

said second controller rewrites said state information corresponding to said data to be processed in order to ~~change the order of executing~~ remove a part of said series of processing ~~functions~~ functions, if it is determined that said data to be processed has a prescribed attribute.

8. (Previously Presented) The data processing system according to claim 1, wherein

said memory has one region to store said state information corresponding to a single region where said data to be processed is stored.

9. (Previously Presented) The data processing system according to claim 1, wherein

said memory has one region to store said state information corresponding to a plurality of regions where said data to be processed is stored.

10. (Canceled)

11. (Previously Presented) A data processing system comprising:

a plurality of processing means for executing a series of processing functions of different types on data to be processed in a prescribed order, each processing means executing a processing function different from one another and said data to be processed being image data that consists of a plurality of pixel data; and

memory means for storing said data to be processed in association with state information to represent the processing to be performed next for each pixel data of said data to be processed, wherein

said processing functions are executed asynchronously on said data to be processed by said plurality of processing means, one processing is executed on each pixel data by one of the processing means at a time, and said plurality of processing means share said memory means.

12. (Original) The data processing system according to claim 11, wherein

said plurality of processing means each determine whether said data to be processed can be processed based on said state information.

13. (Previously Presented) The data processing system according to claim 12, wherein

said plurality of processing means each execute a processing on said data to be processed and then rewrite said state information corresponding to the processed data.

14. (Previously Presented) The data processing system according to claim 11, further comprising first control means for controlling said plurality of processing means to execute said series of processing functions based on said state information.

15. (Previously Presented) The data processing system according to claim 14, wherein

said first control means rewrites said state information corresponding to processed data in response to the completion of each processing by said plurality of processing means.

16. (Previously Presented) The data processing system according to claim 11, further comprising a second control means for determining an attribute of said data to be processed, wherein

if it is determined that said data to be processed has a prescribed attribute, said second control means rewrites said state information corresponding to said data to be processed in order to change the order of executing said series of processing functions.

17. (Previously Presented) The data processing system according to claim 16, wherein

said second control means rewrites said state information corresponding to said data to be processed in order to remove a part of said series of processing functions if it is determined that said data to be processed has a prescribed attribute.

18. (Previously Presented) The data processing system according to claim 11, wherein

said memory means has one region to store said state information corresponding to a single region where said data to be processed is stored.

19. (Previously Presented) The data processing system according to claim 11, wherein

said memory means has one region to store said state information corresponding to a plurality of regions where said data to be processed is stored.

20. (Canceled)

21. (Previously Presented) The data processing system of claim 1 wherein a given data item is stored at the same location in said memory after each of said plurality of processing functions is performed on said given data item.

22. (Previously Presented) The data processing system of claim 21 wherein the state information for said given data item is stored at the same location in said memory after each of said plurality of processing functions is performed on said given data item.

23. (Previously Presented) The data processing system of claim 11 wherein a given data item is stored at the same location in said memory means after each of said plurality of processing functions is performed on said given data item.

24. (Previously Presented) The data processing system of claim 23 wherein the state information for said given data item is stored at the same location

in said memory means after each of said plurality of processing functions is performed on said given data item.

25. (Previously Presented) A data processing device comprising:

a first processor for executing first processing on data to be processed;

a second processor for executing second processing on said data to be processed that was subjected to the first processing; and

a memory for storing said data to be processed in association with state information to represent the processing state of said data, wherein

said first and second processing are asynchronously executed on said data to be processed by said first and second processors and said first and second processors share said memory.

26. (Previously Presented) An image processing device comprising:

a first image processor for executing first image processing on image data;

a second image processor for executing second image processing on said image data that was subjected to the first image processing; and

a memory for storing said image data in association with state information to represent the processing state of said image data, wherein

said first and second image processings are asynchronously executed on said image data by said first and second image processors and said first and second image processors share said memory.